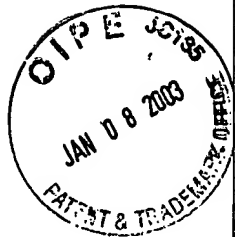


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/903,059 Confirmation No.: 9375
 First Named Inventor: Constantin Bulucea Filing Date: July 10, 2001
 Group Art Unit: 2814 Examiner: Farahani, D.
 Atty. Docket No.: NS-4971 US
 Title: Gate-Enhanced Junction Varactor
 Assignee: National Semiconductor Corporation

#14 He to Drafts
 M. Baurer
 4/9/03

San Jose, California
 January 8, 2003

COMMISSIONER FOR PATENTS
 Washington, D.C. 20231

AMENDMENT TO DRAWINGS

Sir:

The drawings for the above patent application should be amended in the following manner.

In Fig. 10b, after "or," "Decreasing" should be changed to "Increasing".

In Fig. 13, the lead lines for reference symbols "208L" and "208U" should be reversed.

In Fig. 14, the abbreviation "V" for volts should be inserted parenthetically after "Gate-to-Source Voltage V_{GS} " along the horizontal axis of the figure.

In each of Figs. 19b and 23b, reference symbol " V_{SS} " should be changed to " V_{LL} ".

In each of Figs. 24 and 26, the lower lead line extending from reference symbol "138" should be changed to a lower lead line extending from reference symbol "134".

Enclosed are copies of the relevant drawing sheets in which the changes to the foregoing figures are indicated in red.

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